Amendments to the Claims:

Claims 6, 8 and 10 have been amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

Claims 1-5. (Canceled)

6. (Currently Amended) A method of making a transistor on a substrate having a dielectric layer thereon comprising:

forming a gate structure overlying the dielectric layer, the gate structure having a gate oxide layer formed on ~~said~~ the dielectric layer, an adhesion layer formed on the gate oxide layer and a metal silicide layer formed on ~~said~~ the adhesion layer, ~~gate oxide layer, said~~ the gate structure having a first sidewall and a second sidewall, defining a first contact region, a second contact region and a channel region therebetween; and ~~defining a first contact region, a channel region and a second contact region therewithin;~~

forming first, second and third subregions within the ~~second~~ contact regions, each subregion having a dopant concentration that is different from that of the other two subregions, wherein forming said subregions comprises:

introducing a first dopant into the substrate to form a first subregion, the first subregion being generally aligned with the sidewalls of the gate structure;

forming a first single thin layer sidewall spacer of dielectric material overlying the~~said second~~ sidewalls, the ~~said~~ first single thin layer sidewall spacer formed by depositing a thin conformal layer of dielectric material over the ~~said~~ substrate and etching to a predetermined thickness over the~~said second~~ sidewalls;

providing an ~~for an~~ annealing/oxidation step at an elevated temperature;

forming a second single layer sidewall spacer overlying the~~said~~ first single thin layer spacer, the ~~said~~ second single layer sidewall spacer having a thickness greater than the~~said~~ first single thin layer sidewall spacer;

introducing a ~~first~~ second dopant into the substrate to form the~~said~~ ~~first~~ second subregion, the ~~said~~ second~~first~~ subregion being generally aligned with ~~said~~ the second single layer sidewall spacer;

reducing the thickness of the second single layer sidewall spacer to form a third sidewall spacer having a thickness intermediate the~~said~~ first and second sidewall spacers; and

introducing a third~~second~~ dopant into the substrate to form the third~~said second~~ subregion, ~~said second~~the third subregion being generally aligned with the third sidewall spacer.~~;~~

~~substantially removing the third sidewall spacer; and~~

~~introducing a third dopant into the substrate to form said third subregion, said third subregion being generally aligned with said second sidewall.~~

7. (Previously Presented) The method of claim 6, wherein the first single thin layer sidewall spacer is anisotropically etched to a thickness of between about 50 and 150 Angstroms.

8. (Currently Amended) The method of claim 6, wherein the second single layer sidewall spacer is etched to a thickness of about 2 to 20 times the thickness of ~~said~~ the first single thin layer sidewall spacer.

9. (Previously Presented) The method of claim 6, wherein the second single layer sidewall spacer is etched to a thickness of about 550 Angstroms.

10. (Currently Amended) The method of claim 6, wherein ~~said~~ the first single thin layer sidewall spacer is formed of one of silicon nitride and silicon dioxide.